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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/732,545
Filing Date	12/18/2000
First Named Inventor	Dennis A. Barney ET AL.
Group Art Unit	2863
Examiner Name	Demetrius R. Pretlow
Total Number of Pages in This Submission	
Attorney Docket Number	00-216

ENCLOSURES *(check all that apply)*

- [X] Fee Transmittal Form
  - [X] Fee Attached
- [ ] Amendment / Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Assignment Papers *(for an Application)*
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
- [ ] After Allowance Communication to Group
- [ ] Appeal Communication to Board of Appeals and Interferences
- [X] Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- [ ] Proprietary Information
- [ ] Status Letter
- [ ] Other Enclosure(s) *(please identify below)*:

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Robin S. Fahlberg, Registration No. 50,393
Signature	Robin S. Fahlberg
Date	September 19, 2003

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope address to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 on this date: 09/19/2003

Typed or printed name	Robin S. Fahlberg		
Signature	Robin S. Fahlberg	Date	9/19/2003

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FEE TRANSMITTAL for FY 2003

Effective 01/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 320

Complete if Known	
Application Number	09/732,545
Filing Date	12/18/2000
First Named Inventor	Dennis A. Barney ET AL.
Examiner Name	Demetrius R. Pretlow
Art Unit	2863
Attorney Docket No.	00-216

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit Card ☐ Money Order ☐ Other ☐ None

☒ Deposit Account

Deposit Account Number: 03-1129

Deposit Account Name:

The Commissioner is authorized to: *(check all that apply)*

☒ Charge fee(s) indicated below ☒ Credit any overpayments

☐ Charge any additional fee(s) during the pendency of this application

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	750	2001	375	Utility filing fee	
1002	330	2002	165	Design filing fee	
1003	520	2003	260	Plant filing fee	
1004	750	2004	375	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 0

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims		Fee from below		Fee Paid
Total Claims		-20** =		X		=	
Independent Claims		- 3** =		X		=	
Multiple Dependent						=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2002	9	Claims in excess of 20
1201	84	2001	42	Independent claims in excess of 3
1203	280	2203	140	Multiple dependent claim, if not paid
1204	84	2204	42	**Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

***or number previously paid, if greater; For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a reqeust for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	410	2252	205	Extension for reply within second month	
1253	930	2253	465	Extension for reply within third month	
1254	1,450	2254	725	Extension for reply within fourth month	
1255	1,970	2255	985	Extension for reply within fifth month	
1401	320	2401	160	Notice of Appeal	
1402	320	2402	160	Filing a brief in support of an appeal	320
1403	280	2403	140	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,300	2453	650	Petition to revive - unintentional	
1501	1,300	2501	650	Utility issue fee (or reissue)	
1502	470	2502	235	Design issue fee	
1503	630	2503	315	Plant issue fee	
1460	130	1460	130	Petitions to the Commisioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	750	2809	375	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	750	2810	375	For each additional invention to be examined (37 CFR 1.129(b))	
1801	750	2801	375	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 320

SUBMITTED BY

(Complete *(if applicable)*)

Name (Print/Type)	Robin S. Fahlberg	Registration No. (Attorney/Agent)	50,393	Telephone	(309) 675-5682
Signature	Robin S. Fahlberg			Date	09/19/2003

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	)	
	)	
Dennis A. Barney, etal.	)	Art Unit: 2863
	)	
Application No. 09/732,545	)	Examiner: Demetrius R. Pretlow
	)	
Filed: December 18, 2000	)	Paper No.: 9
	)	
For: A METHOD AND APPARATUS OF MANAGING TIME FOR A PROCESSING SYSTEM	)	
	)	
Attorney Docket No. 00-216	)	

Peoria, Illinois 61629-6490

September 19, 2003

Honorable Commissioner of
Patents and Trademarks
Alexandria, VA 22313-1450

APPELLANTS' BRIEF IN SUPPORT OF APPEAL FROM THE PRIMARY EXAMINER TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Sir:

This Brief in support of Appellant's Notice of Appeal is being submitted in triplicate pursuant to 37 C.F.R. 1.192. Please charge deposit account No. 03-1129 the filing fee of $310.00 as specified in 37 C.F.R. 1.17(c) and any other charges required for the filing of this brief. Claims 1-38 are attached hereto in Appendix A, pursuant to 37 C.F.R. 1.192(c)(9).

Real Party in Interest

Caterpillar Inc. is the assignee of the present application and, therefore, is the real party in interest in the present appeal.

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10/21/2003 SLUANG1 00000007 09732545
01 FC:1402 320.00 DA

Related Appeals and Interferences

There are no other pending appeals or interferences related to the application that is the subject of this appeal. Further, Appellant has no knowledge of any appeals or interferences which would have an effect on the present appeal.

Status of Claims

Claims 1-38 are pending in the application that is the subject of this appeal. The Examiner finally rejected claims 1-38 in the Office Action dated April 21, 2003. Appellant is appealing the rejection of claims 1-38.

Status of Amendments

Appellant has not filed an amendment subsequent to the final rejection dated April 21, 2003.

Summary of Invention

The present invention relates generally to time management, and more particularly, to a method and apparatus of managing time for a processing system located on a machine. (Page 1, Lines 7-10).

Time management on a machine, such as an earth moving machine, is an important task. Time management on multi-processor systems is needed both for coordinated event logging, and also to ensure the controllers perform coordinated tasks at the appropriate time. Some systems attempt to have all of the controllers operate in lock step with each other. The system may utilize one clock, located on a controller, such as a master controller. The master controller may determine the time and distribute the time to the other controllers. Without a local clock, the other controllers have no concept of time except what is delivered to them from the master controller. Therefore, keeping time with a desired resolution places a burden on the communication network. In addition, failures such as to the communication network or master controller, either temporary or long term, disrupts time management for

the system because time updates are not performed. Therefore, time management is ineffective when failures occur. (Page 1, lines 13-30, Page 2, lines 1-4)

The present invention includes a method and apparatus of managing time for a processing system located on a machine. The processing system includes a plurality of controllers and a communication network connecting each of the controllers. Each of the controllers has a local clock. The method includes the steps of establishing an operating characteristic of the machine, determining whether to update a local time in response to said operating characteristic, and updating said local time based upon the local clock in response to said update determination. (Specification Abstract).

Issues

1. Whether the Examiner erred in rejecting claims 1-38 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,012,004 issued to Sugano et al. (hereafter referred to as "Sugano").

Grouping of Claims

The Examiner's grounds for rejection applied to more than one claim in Issue 2 and Issue 4. With respect to each of the rejections, Appellants group the claims as follows:

1. Claims 1-8, 15 and 25-33 stand together.
2. Claims 9-14, 16-24 and 34-38 stand together.

Argument

I. **The Examiner erred in rejecting claims 1-38 under 35 U.S.C. § 102(e) as being anticipated by Sugano as the reference does not teach or suggest each and every limitation of Appellants' claims 1-38.**

A. Claims 1-8, 15 and 25-33

At a minimum, Sugano does not teach or suggest Appellants' claim limitations of "each controller having a clock" (in claim preamble) and "updating said local time using the local clock in response to said update determination."

In the Official Action dated April 25, 2002, the Examiner rejected claims 1-38 under 35 U.S.C. §102(e) and argued that the claim limitation of "updating said local time using the local clock in response to said update determination." contained in Appellants' claim limitations was taught in Sugano in column 2, lines 38-44 and claim 9, lines 1-8. In response to the Official Action, Appellants pointed out that column 2, lines 38-44 of Sugano described prior art, that neither this prior art nor Sugano taught the claim limitation, and that it was improper to combine parts of two separate embodiments to allege the claim limitation was disclosed. Apparently the Examiner agreed because the 35 U.S.C. §102(e) rejection was withdrawn in the Official Action dated November 6, 2002.

In the Official Action dated November 6, 2002, the Examiner admits that "Sugano et al does not teach a plurality of controllers having a local clock and a communication network." or "updating the local time using the local clock in response to the update determination.", but argues for a 35 U.S.C. §103(a) rejection based on Sugano in view of U.S. Patent No. 6,236,277-B1 to Esker (hereafter referred to as "Esker"). Appellants argued there was no motivation to combine and that Sugano teaches away from the combination. Apparently the Examiner agreed as that rejection was withdrawn in the Official Action dated April 21, 2003.

In the Official Action dated April 21, 2003, the Examiner seems to have changed his mind and now asserts that Sugano does disclose "a plurality of controllers having

a local clock and a communication network." and "updating the local time using the local clock in response to the update determination." Appellants respectfully disagree.

The *Comprehensive Dictionary of Electrical Engineering* (CRC Press, 1999, Boca Raton, FL), defines clock as "the oscillator circuit that generates a periodic synchronization signal" or "a circuit that provides a series of electrical pulses at regular intervals that can be used for timing or synchronization purposes."

The Examiner contends that Sugano teaches a plurality of controllers having a CPU which inherently has some type of clock and a communication network. Appellants agree, but point out that the clock is contained only in the master controller and not in the other controllers. The other controllers do not contain clocks, but receive the time from the master controller and store the time in a local storage space for reference.

The Examiner now contends that Sugano teaches "updating the local clock in response to the update determination" at column 5, lines 49-53 and column 8, lines 29-46. Column 5, lines 49-53 read:

> The controller 8 of each of the controllers 11 receives the main standard time value, and renews its own secondary time storage means.

Column 8, lines 29-46 reads:

> Since one renewal unit time has elapsed from the preceding processing, the secondary standard time is equalized to the main standard time, and the procedure advances to step 122.
>
> Step122
>
> The renewed secondary standard time, secondary operating time, and exchange time are written in each of the predetermined storage areas of the memory 14 to complete the processing.
>
> In this way, when the main standard time is renewed by one renewal unit time, the CPU renews the secondary standard time, the secondary operating time, and the exchange time, stored in each of the controllers 11, based on the new standard time. Therefore, since these times are uniformly renewed by the main standard time of the master controller 1, time errors between the controllers 11 are eliminated.

It would seem that the Examiner has confused storage areas in controllers for storing time measured and transmitted by the master controller with local clocks.

Not only does Sugano not teach or disclose local clocks, it actually teaches away from them. As pointed out in Appellants' Response to the Official Action of November 6, 2002, "Sugano discloses an invention to overcome the problems in the prior art of multiple clocks with an invention that has only one clock, that in the master controller. The master

controller transmits a counted time to a plurality of controllers as a standard time, thus eliminating the need for individual clocks in the other controllers and creating and transmitting a standard time determined by the master controller clock and stored in the memories of the other controllers."

In light of the foregoing arguments, Appellant respectfully submits that the Examiner's rejection of claims 1-8, 15 and 25-33 under 35 U.S.C. §102(e) as anticipated by Sugano was improper.

B. Claims 9-14, 16-24 and 34-38

Sugano further fails to disclose the limitations in Appellant's claims 9-14, 16-24 and 34-38 "wherein the step of establishing said master controller further comprises the step of participating in an arbitration process among the controllers." In the Official Action of April 21, 2003, the Examiner admits that Sugano "does not explicitly teach the master controller participating in an arbitration process among the controllers". But, the Examiner contended that "the arbitration process which includes receiving the arbitration signal would be inherent to the system of Sugano et al. Note column 5, lines 43-47." Appellants respectfully disagree.

Sugano column 5, lines 43-47 states:

> Therefore, the master controller 1 is not limited thereto, and any one of the plurality of controllers 11 in the vehicle control apparatus can be selected as a master controller, and the standard time counting means 9 can be provided in that controller.

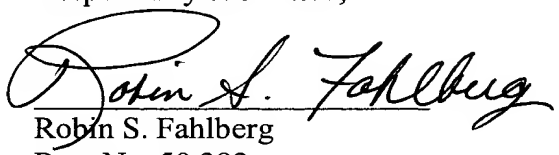
Because the standard time counting means has to be provided in the master controller, an arbitration process is not inherent. There can be only one master controller, the one with the standard time counting means. The master controller can be established through hardware or software to always be the master controller with no arbitration process necessary. Thus, the arbitration process is not inherent.

In light of the foregoing arguments, Appellant respectfully submits that the Examiner's rejection of claims 9-14, 16-24 and 34-38 under 35 U.S.C. §102(e) as anticipated by Sugano was improper.

Conclusion

Appellants respectfully request the Board to reverse the Examiner's final rejection of the claims pending in the present application and to order the allowance of those claims.

Respectfully submitted,



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Appendix A

Claims Involved in the Appeal

Claims

1. A method of managing time for a controller located in a processing system on a machine, the processing system including a plurality of controllers, each controller having a local clock, and a communication network connecting each of the controllers, including the steps of:

establishing an operating characteristic of the machine;

determining whether to update a local time in response to said operating characteristic; and

updating said local time using the local clock in response to said update determination.

2. A method, as set forth in claim 1, further comprising the steps of:

receiving an official time;

determining a difference between said official time and said local time; and,

determining whether to synchronize said local time with said official time in response to said time difference.

3. A method, as set forth in claim 2, wherein the step of establishing said operating characteristic further comprises the step of receiving an operating characteristic, said operating characteristic being indicative of the machine being operated.

4. A method, as set forth in claim 2, wherein the step of establishing said operating characteristic further comprises the step of receiving an operating characteristic, said operating characteristic being indicative of the engine being operated.

5. A method, as set forth in claim 2, wherein the step of determining whether to synchronize said local time further comprises the step of determining to synchronize said local time with said official time in response to said time difference being greater than a first threshold.

6. A method, as set forth in claim 5, further comprising the step of establishing a master controller of the processing system.

7. A method, as set forth in claim 6, wherein the step of receiving said official time further comprises the step of receiving said official time from said master controller.

8. A method, as set forth in claim 7, wherein the step of establishing said operating characteristic further comprises the step of receiving an operating characteristic signal from said master controller.

9. A method, as set forth in claim 6, wherein the step of establishing said master controller further comprises the step of participating in an arbitration process among the controllers.

10. A method, as set forth in claim 9, further comprising the step of receiving an arbitration signal.

11. A method, as set forth in claim 10,

generating a priority signal in response to receiving said arbitration signal, said priority signal being indicative of at least one controller characteristic.

12. A method, as set forth in claim 11, further comprising the steps of:

receiving at least one priority signal;

determining whether to become the master controller in response to said received at least one priority signal.

13. A method, as set forth in claim 10, further comprising the step of initiating said arbitration process in response to receiving power.

14. A method, as set forth in claim 10, wherein the step of initiating said arbitration further comprises the step of initiating said arbitration process in response to failing to receive one of said official time and said operating characteristic.

15. An apparatus configured to manage time on a processing system located on a machine, comprising:

a plurality of controllers;

a local clock located on each controller and configured to establish a local time;

a communication network connected to said controllers; and

wherein each of said plurality of controllers is configured to establish an operating characteristic of the machine, determine whether to update said local time, using said local clock, in response to said operating characteristic, and updating said local time in response to said update determination.

16. An apparatus, as set forth in claim 15, wherein said plurality of controllers being further adapted to establish a master controller in response to an arbitration process, the remaining controllers being non-master controllers.

17. An apparatus, as set forth in claim 16, wherein each of said non-master controllers receives an official time signal from said master controller.

18. An apparatus, as set forth in claim 17, wherein each of said non-master controllers is further adapted to determine a difference between said official time and said local time and determine whether to synchronize said local time with said official time in response to said time difference.

19. An apparatus, as set forth in claim 18, wherein each of said non-master controllers receives an operating characteristic signal, indicative of said operating characteristic, from said master controller.

20. An apparatus, as set forth in claim 19, wherein said operating characteristic is indicative of at least one of a machine operation and an engine operation.

21. An apparatus, as set forth in claim 20, wherein each of said non-master controllers is further adapted to synchronize said local time with said official time in response to said difference being greater than a first threshold.

22. An apparatus, as set forth in claim 21, wherein at least one of said non-master controllers initiates said arbitration in response to failing to receive one of said official time signal and said operating characteristic signal.

23. An apparatus, as set forth in claim 22, wherein each said non-master controller generates a priority signal indicative of said controllers capability.

24. An apparatus, as set forth in claim 23, wherein each said non-master controller is further adapted to determine whether to be the master controller in response to receiving said priority signals.

25. A method of managing time for a processing system located on a machine, the processing system including a plurality of controllers, each controller having a local clock, and a communication network connecting each of the controllers, including the steps of:

establishing an operating characteristic of the machine;

determining whether to update a local time on each of the controllers in response to said operating characteristic; and

updating said local time, using the local clock, in response to said update determination.

26. A method, as set forth in claim 25, further comprising the steps of:

establishing an official time;

determining a difference between said official time and said local time; and,

determining whether to synchronize said local time with said official time in response to said time difference.

27. A method, as set forth in claim 26, further comprising the step of establishing a master controller, the other controllers being non-master controllers.

28. A method, as set forth in claim 27, wherein the step of establishing said operating characteristic further comprises the step of delivering an operating characteristic to each of the non-master controllers, said operating characteristic being indicative of the machine being operated.

29. A method, as set forth in claim 27, wherein the step of establishing said operating characteristic further comprises the step of delivering an operating characteristic signal to each of the non-master controllers, said operating characteristic being indicative of the engine being operated.

30. A method, as set forth in claim 27, wherein the step of determining whether to synchronize said local time further comprises the step of synchronizing said local time with said official time in response to said time difference being greater than a first threshold.

31. A method, as set forth in claim 30, wherein the step of receiving said official time further comprises the step of receiving said official time from said master controller.

32. A method, as set forth in claim 31, wherein the step of establishing said operating characteristic further comprises the step of receiving an operating characteristic signal from said master controller.

33. A method, as set forth in claim 32, wherein the step of establishing said master controller further comprises the step of arbitrating among the controllers.

34. A method, as set forth in claim 33, wherein the step of arbitrating further comprises the steps of:

at least one of the controllers initiating said arbitration; and

said at least one controller generating an arbitration signal in response to said intitiation.

35. A method, as set forth in claim 34, further comprising the step of generating a priority signal in response to receiving said arbitration signal, said priority signal being indicative of at least one controller characteristic.

36. A method, as set forth in claim 35, further comprising the steps of:

receiving said priority signals;

determining whether to become the master controller in response to said received priority signals.

37. A method, as set forth in claim 36, wherein the step of initiating said arbitration further comprises the step of initiating said arbitration process in response to receiving power.

38. A method, as set forth in claim 37, wherein the step of initiating said arbitration further comprises the step of initiating said arbitration process in response to failing to receive one of said official time and said operating characteristic.